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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,939	08/23/2001	Robert Edward Galbraith	IBM / 67DV1	1833

7590 12/19/2003

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	18

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,939	GALBRAITH ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-30 and 45-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-30 and 45-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed October 24, 2003 in response to PTO Office Action dated July September 4, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 21-30, and 45-57 have been presented for examination in this application. In response to the last Office Action, claims 21, 45, and 55 have been amended.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-30, 46, 47, and 55-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21 and 55 recite, "storing, in a cache memory having a total usable hardware memory capacity for a DASD cache..." in lines 4-5 and 5-6, respectively. It is unclear to the Examiner whether the "a cache memory" corresponds to the "DASD cache". If this correspondence is correct, the Examiner encourages the Applicant to modify claims 21 and 55 to incorporate language akin to that of claim 45, which recites

"...a DASD cache memory having a total usable hardware memory capacity..." in lines 3-4.

Claim 22 recites the limitation "the total cache memory capacity" in line 2. There is insufficient antecedent basis for this limitation in the claim. The limitation "total cache memory capacity" had not been previously recited.

Claim 23 recites the limitation "the total cache memory capacity" in line 2. There is insufficient antecedent basis for this limitation in the claim. The limitation "total cache memory capacity" had not been previously recited.

Claim 46 recites the limitation "the total cache memory capacity" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. The limitation "total cache memory capacity" had not been previously recited.

Claim 22 recites the limitation "the total cache memory capacity" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. The limitation "total cache memory capacity" had not been previously recited.

Claims 24-30, 48-54, 56, and 57 are rejected as being dependent upon a previously rejected claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The following 35 U.S.C. 103(a) rejections are made in light of the preceding 35 U.S.C. 112, second paragraph rejections.

Claims 21 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cord et al. (US# 5,627,990) in view of Santeler et al. (US# 6,430,702).

Cord et al. teaches a **DASD caching management system** including a number of logical **DASD** storage devices and a **storage controller (24)** that contains **cache controller memory (50)** with multiple memory locations for storing data (col. 5, lines 36-44 & col. 6, lines 8-12). **Hardware cache (50) modules** store **data retrieved** from the DASD (col. 7, lines 9-10 & 41-54; col. 1, lines 45-50). Cord et al. further teaches **cache directories** to reflect and **identify** the contents of the cache memory (col. 3, lines 15, 39-41, & 50-52). Responding to a request for a **copy of data from a DASD,** where the data **is in the cache**, a 'read hit' occurs and the data is **accessed and transferred** from the cache memory. Responding to a request for a **copy of data from a DASD,** where the data **is not in the cache**, a 'read miss' occurs and the data is **accessed and transferred** from the DASD to the cache memory.

The difference between the claimed subject matter and that of Cord et al. is that the claims recite altering the cache directory according to a change in total usable hardware cache memory capacity. Santeler et al. teaches a fault tolerant memory system where **memory modules may be "hot swapped", referring to memory expansion or reduction, while the system remains powered up** (col. 2, lines 24-30; col. 3, lines 49-52 & 58-60). This "hot swapping" feature would constitute **a change in the total usable hardware**. Santeler et al. further teaches that a memory controller

divides the physical address space of the memory modules into multiple data banks, including redundant and level-4 RAID memory banks. Each stripe of the level-4 RAID represents a contiguous block of data that is transferred to/from the memory modules. Each of the stripe regions are **mapped into the address spaces of several memory modules** (col. 3, lines 60-67; col. 4, lines 19-34, 37-44, and 54-57). Although not specifically recited by Santeler et al., the memory module system of Santeler et al. would inherently contain a **directory or table** in order to facilitate the storage of the logical to physical-to-physical memory mappings as recited above. Also, since Santeler et al. teaches the addition and removal of memory modules in combination with the RAID mapping system, the memory mappings would inherently require **modification, or altering**, should one of the modules be removed or added. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Cord et al. and Santeler et al. before him at the time the invention was made to modify the cache management system of Cord et al. to include the fault tolerant memory module system of Santeler et al., because then multiple memory module failures could be tolerated, system crashes prevented, and the swapping of memory modules included as taught by Santeler et al. (col. 2, lines 24-30).

Claims 22-24, 46-48, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cord et al. (US# 5,627,990) in view of Santeler et al. (US# 6,430,702) as applied to claims 21 and 45 above, and further in view of McNutt et al. (US# 5,649,153).

The difference between the claimed subject matter and the already modified invention of Cord et al. with the teaching of Santeler et al., disclosed supra, is that claims 22, 23, 46, and 47 recite cache directory updating based upon the increasing and decreasing of the cache size.

The following applies in general to claims 22, 23, 46, and 47. The reference of McNutt et al. teaches a similar field of invention including a DASD caching management system. A cache (205) stores data pulled from the DASD drives (209).

A cache directory (219) attached to the cache used to detail what data has been read into the cache from the DASD drives, such that **the directory maintains a listing of where the data is stored in the cache** (col. 3, lines 51-53 & 59-62). As data is added and removed from the cache, the amount of cache space available inherently alters, or affects, the number of data listings in the cache directory. Thus, the total available memory capacity (amount of cache space available) for the cache changes for every write operation into the cache, for example, and the cache directory is altered, or updated, to reflect the change in total memory capacity.

Regarding claims 22 and 46, when data is added to the cache, **the cache directory includes its associated directory listing**. Thus, the new directory listing

would **contain more directory entries** and portray a **diminished amount of cache space that is available for use**. Should data need to be pulled from a DASD drive, the controller (203) checks the directory for available space for the data to be placed into the cache.

Regarding claims 23 and 47, when data is removed from the cache, **the cache directory removes its associated directory listing**. Thus, the new directory listing would **contain fewer directory entries** and portray an even **greater amount of cache space that is available for use**. Should data need to be pulled from a DASD drive, the controller (203) checks the directory for available space for the data to be placed into the cache.

The difference between the claimed subject matter and that of Cord et al. and Santeler et al., disclosed supra, is that claims 24 and 48 recite monitoring data access to data stored in the cache memory.

Regarding claims 24 and 48, the caching system of McNutt et al. teaches **monitoring data accesses to data stored in the cache** (col. 4, lines 56-58).

The difference between the claimed subject matter and that of Cord et al. and Santeler et al., disclosed supra, is that claims 30 and 54 recite monitoring data access to data not stored in the cache memory.

Regarding claims 30 and 54, the caching system of McNutt et al. also teaches **monitoring data accesses to data not currently stored in the cache** (col. 5, lines 24-55).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Cord et al., Santeler et al., and McNutt et al. before him at the time the invention was made to modify the cache management system of Cord et al. and Santeler et al. to include the adaption algorithm for data storage of McNutt et al., because then controller (203), which controls the data storage functions of cache (205), can individually adapt its caching behavior based on cache access characteristics without host system software support (col. 3, lines 50-56), as taught by McNutt et al.

Claims 25 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cord et al. (US# 5,627,990) in view of Santeler et al. (US# 6,430,702) and McNutt et al. (US# 5,649,153), as applied to claims 22-24, 46-48, 30, and 54 above, and further in view of Mayfield (US# 5,737,565).

Cord et al. teaches that the cache memory uses normal caching algorithms including LRU, where data remains in the memory until LRU algorithms permit them to be overwritten by other data (col. 9, lines 37-43) according to their associated **LRU ordered value**.

The difference between the claimed subject matter and Cord et al., Santeler et al., and McNutt et al., disclosed supra, is that the claim recites that monitoring data

accesses is done in connection with and LRU queue. Mayfield teaches **monitoring a sequence of cache misses (accesses)**, whereupon that an **LRU filter queue** (502) is used in conjunction with the monitoring step (abs.; Figure 5). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Cord et al., Santeler et al., McNutt et al. and Mayfield before him at the time the invention was made to modify the caching system of Cord et al., Santeler et al., and McNutt et al. to include the LRU queue and scheme of Mayfield, because then items are removed based upon potential access latency and hit ratios in order to speed up data processing, as taught by Mayfield (abs.; col.2, lines 27-53).

Claims 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cord et al. (US# 5,627,990) in view of Santeler et al. (US# 6,430,702) and Tanenbaum.

Cord et al. teaches a **DASD caching management system** including a number of logical **DASD** storage devices and a **storage controller (24)** that contains **cache controller memory (50)** with multiple memory locations for storing data (col. 5, lines 36-44 & col. 6, lines 8-12). **Hardware cache (50) modules** store **data retrieved** from the DASD (col. 7, lines 9-10 & 41-54; col. 1, lines 45-50). Cord et al. further teaches **cache directories** to reflect and **identify** the contents of the cache memory (col. 3, lines 15, 39-41, & 50-52). Responding to a request for a **copy of data from a DASD,** where the data **is in the cache**, a 'read hit' occurs and the data is **accessed and transferred** from the cache memory. Responding to a request for a **copy of data from**

a DASD, where the data **is not in the cache**, a 'read miss' occurs and the data is **accessed and transferred** from the DASD to the cache memory.

A difference between the claimed subject matter and that of Cord et al. is that the claims recite altering the cache directory according to a change in total usable hardware cache memory capacity. Santeler et al. teaches a fault tolerant memory system where **memory modules may be "hot swapped", referring to memory expansion or reduction, while the system remains powered up** (col. 2, lines 24-30; col. 3, lines 49-52 & 58-60). This "hot swapping" feature would constitute **a change in the total usable hardware**. Santeler et al. further teaches that a memory controller divides the physical address space of the memory modules into multiple data banks, including redundant and level-4 RAID memory banks. Each stripe of the level-4 RAID represents a contiguous block of data that is transferred to/from the memory modules. Each of the stripe regions are **mapped into the address spaces of several memory modules** (col. 3, lines 60-67; col. 4, lines 19-34, 37-44, and 54-57). Although not specifically recited by Santeler et al., the memory module system of Santeler et al. would inherently contain a **directory or table** in order to facilitate the storage of the logical to physical-to-physical memory mappings as recited above. Also, since Santeler et al. teaches the addition and removal of memory modules in combination with the RAID mapping system, the memory mappings would inherently require **modification, or altering**, should one of the modules be removed or added.

A difference between the claimed subject matter and that of Cord et al. is that the claims recite that the caching operation functions according to a **program product**.

Tanenbaum teaches that hardware and software are logically equivalent, and that any operation performed by one can also be executed by the other (page 11). Tanenbaum also recites that the software can be represented and stored on **recordable media**, such as recordable magnetic tape media (claims 55 and 57). Regarding claim 56, the **transmission type media** as claimed and described as communications links in the specification relates to communication buses and I/O hardware needed for reading such recordable media as the magnetic tape media. Although not explicitly stated by Tanenbaum, such buses and I/O hardware would be inherent to a computer system implementing recordable tape and other recordable media drives.

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Cord et al., Santeler et al., and Tanenbaum before him at the time the invention was made to modify the cache management system of Cord et al. to include the fault tolerant memory module system of Santeler et al., because then multiple memory module failures could be tolerated, system crashes prevented, and the swapping of memory modules included, as taught by Santeler et al. (col. 2, lines 24-30). The modification of the caching system of Cord et al. to include the software implementation of Tanenbaum would result in a decrease in hardware material costs (page 11).

Allowable Subject Matter

Claims 26-29 and 50-53 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant responded in the Response of October 24, 2003, that "The Examiner indicated at the interview that the claims are allowable over the prior art". The Examiner would like to point out that the Examiner indicated to the Applicant that the amendments to claims 21, 45, and 55 would render the previous rejections moot but did not indicate that the claims were allowable over the prior art. The Examiner had not searched and examined the Application according to the proposed claim amendments, and indicated that a further search and examination would be required.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related "hot swappable" memory and memory allocation systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

December 8, 2003